TEMIC

Siliconix

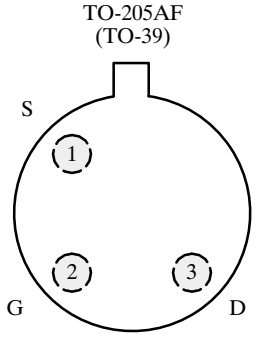
2N6849

P-Channel Enhancement-Mode Transistor

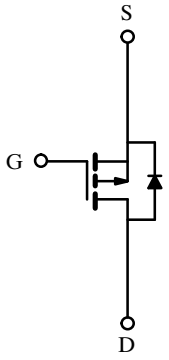
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.30	−6.5

Parametric limits in accordance with MIL-S-19500/564 where applicable.



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−6.5	A
	T_C = 100°C		−3.1	
Pulsed Drain Current		I_{DM}	−25	
Avalanche Current		I_{AR}	−3.1	
Maximum Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R_{thJA}	175	°C/W
Maximum Junction-to-Case	R_{thJC}	5.0	

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Specifications (T_J = 25°C Unless Otherwise Noted)

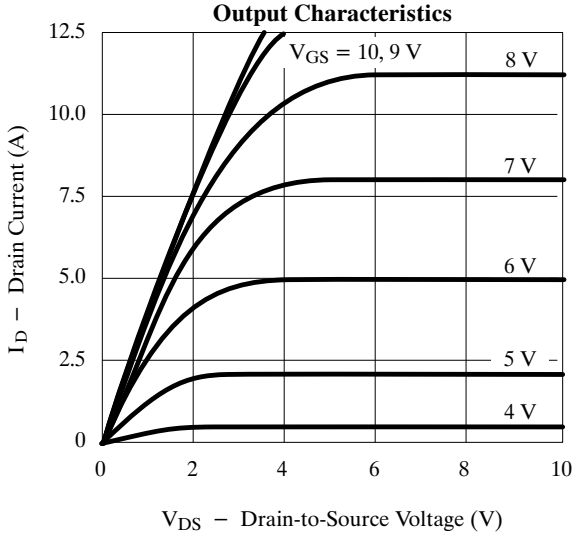
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −1000 µA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −2.1 V, V_{GS} = −10 V	−6.5			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.1 A		0.25	0.30	Ω
		V_{GS} = −10 V, I_D = −4.1 A, T_J = 125°C		0.40	0.54	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −4.1 A	2.5	2.8	7.5	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		625		pF
Output Capacitance	C_{oss}			280		
Reverse Transfer Capacitance	C_{rss}			105		
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −6.5 A	14.7	24	34.8	nC
Gate-Source Charge[c]	Q_{gs}		0.8	3.4	6.8	
Gate-Drain Charge[c]	Q_{gd}		2.0	13.5	23.1	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 10 Ω I_D ≅ −4.1 A, V_{GEN} = −10 V, R_G = 7.5 Ω		9	60	ns
Rise Time[c]	t_r			50	140	
Turn-Off Delay Time[c]	$t_{d(off)}$			32	140	
Fall Time[c]	t_f			38	140	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−6.5	A
Pulsed Current	I_{SM}				−25	
Diode Forward Voltage[b]	V_{SD}	I_F = −6.5 A, V_{GS} = 0 V	−0.8		−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −6.5 A, di/dt = 100 A/µs		110	250	ns
Reverse Recovery Charge	Q_{rr}			0.4		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

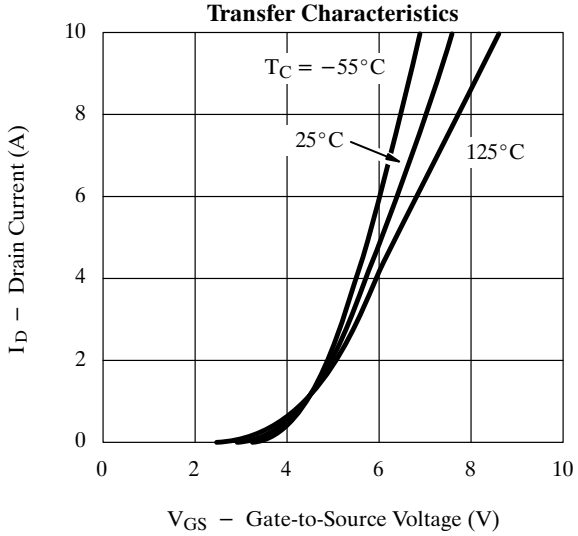
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

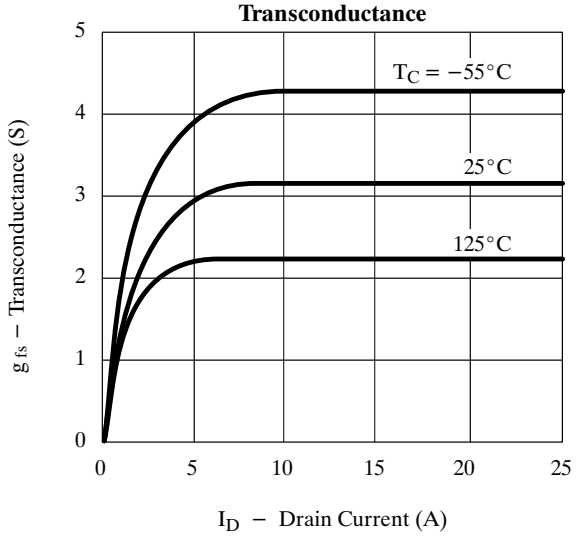
Output Characteristics



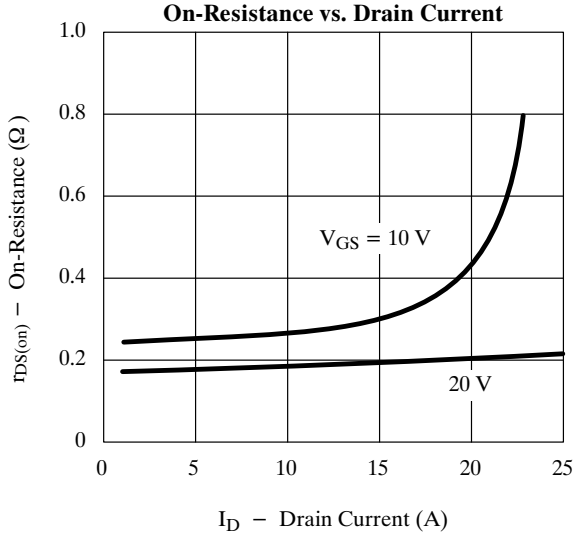
Transfer Characteristics



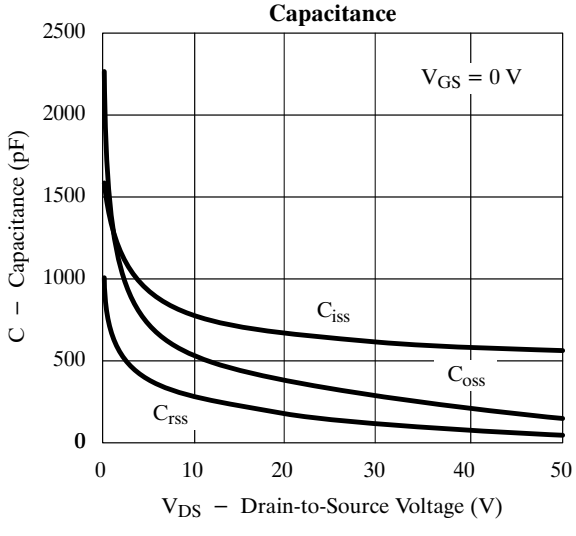
Transconductance



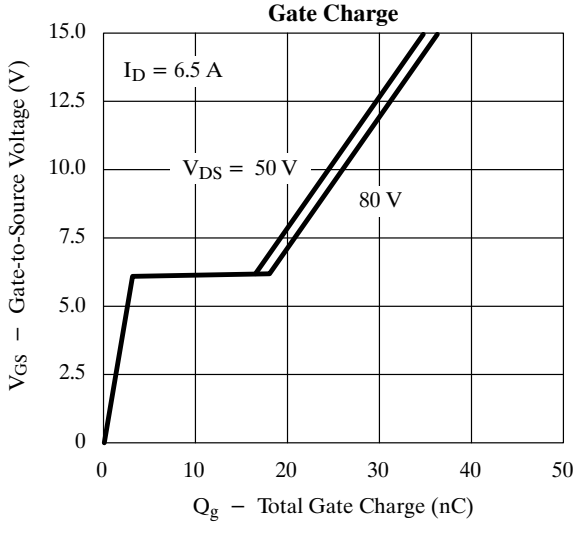
On-Resistance vs. Drain Current



Capacitance



Gate Charge



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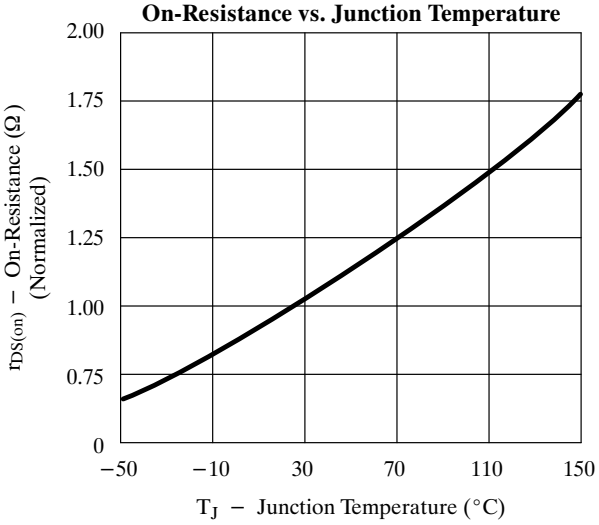
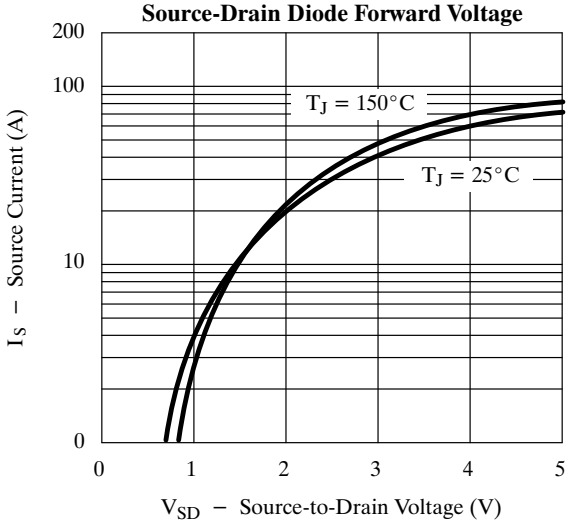
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

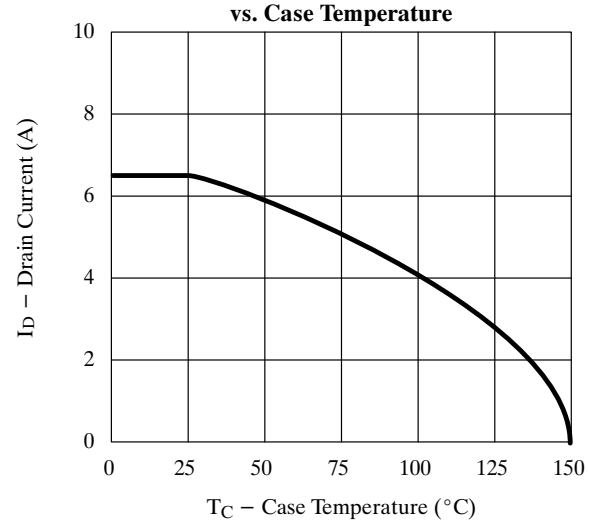


Source-Drain Diode Forward Voltage

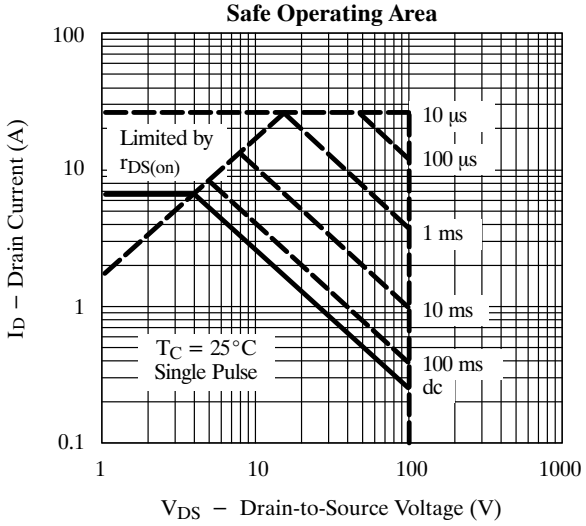


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case